

CLAIMS

What is claimed is:

- 1 1. A method of forming an integrated circuit chip having at least one opening
2 in a substrate, said method comprising:
3 forming an opening having vertical walls in said substrate;
4 protecting a first portion of said vertical walls of said opening, leaving a
5 second portion of said vertical walls unprotected; and
6 laterally patterning said second portion of said opening to change a
7 property of said opening.
- 1 2. The method in claim 1, wherein said laterally patterning comprises one of
2 an isotropic wet etch, an isotropic dry etch and an anisotropic wet etch.
- 1 3. The method in claim 1, wherein said protecting comprises forming a mask
2 over said first portion of said vertical walls.
- 1 4. The method in claim 1, wherein said first portion comprises one of an
2 upper and a lower portion of said opening.

1 5. The method in claim 1, wherein said first portion and said second portion
2 comprises alternating portions along a length of said opening.

1 6. A method of forming an integrated circuit chip having at least one opening
2 in a substrate, said method comprising:

3 forming an opening having vertical walls in said substrate;

4 protecting a first portion of said vertical walls of said opening, leaving a
5 second portion of said vertical walls unprotected; and

6 laterally patterning said second portion of said opening to form a step in
7 said opening.

1 7. The method in claim 6, wherein said laterally patterning comprises one of
2 an isotropic wet etch, an isotropic dry etch and an anisotropic wet etch.

1 8. The method in claim 6, wherein said protecting comprises forming a mask
2 over said first portion of said vertical walls.

1 9. The method in claim 6, wherein said first portion comprises a lower
2 portion of said opening.

1 10. The method in claim 6, wherein said substrate comprises a semiconductor
2 and said method further comprises doping selected portions of said step to form
3 two conductive regions separated by a semiconductive region,

4 wherein in the presence of an adjacent voltage field, said semiconductive
5 region changes its conductivity and performs a switching operation in
6 combination with said conductive regions.

1 11. A method of forming an integrated circuit chip having at least one
2 transistor, said method comprising:

3 forming an opening having vertical walls in a semiconductor substrate;
4 protecting a first portion of said vertical walls of said opening, leaving a
5 second portion of said vertical walls unprotected;

6 laterally patterning said second portion of said opening to form a step in
7 said opening; and

8 doping selected portions of said step to form two conductive regions
9 separated by a semiconductive region,

10 wherein in the presence of an adjacent voltage field, said semiconductive
11 region changes its conductivity and performs a switching operation in
12 combination with said conductive regions.

1 12. The method in claim 11, wherein said laterally patterning comprises one of
2 an isotropic wet etch, an isotropic dry etch and an anisotropic wet etch.

1 13. The method in claim 11, wherein said protecting comprises forming a
2 mask over said first portion of said vertical walls.

1 14. The method in claim 11, wherein said first portion comprises a lower
2 portion of said opening.

1 15. A method of forming an integrated circuit chip having at least one opening
2 in a substrate, said method comprising:

3 forming an opening having vertical walls in said substrate;
4 protecting first portions of said vertical walls of said opening, leaving
5 second portions of said vertical walls unprotected, wherein said first portions
6 alternate with said second portions; and
7 laterally patterning said second portions of said opening to change a
8 property of said opening.

1 16. The method in claim 15, wherein said laterally patterning comprises one of
2 an isotropic wet etch, an isotropic dry etch and an anisotropic wet etch.

1 17. The method in claim 15, wherein said protecting comprises forming a
2 mask over said first portions of said vertical walls.

1 18. The method in claim 15, further comprising, after said laterally patterning,
2 lining said opening with an insulator and filling a remainder of said opening with
3 a conductor to form a deep trench capacitor.

1 19. The method in claim 15, further comprising, after said laterally patterning:
2 forming a gate insulator in said second portions;
3 forming a gate conductor over said gate insulator in said second portions;
4 doping said first portions to form source and drain regions; and
5 forming isolation regions over said source and drain regions.

1 20. The method in claim 19, wherein said gate insulator, said gate conductor,
2 said source and drain regions and said isolation regions comprise a vertical
3 transistor.

4 21. An integrated circuit having at least one trench capacitor, said trench
5 capacitor comprising:
6 an opening having vertical sides, said vertical sides including a plurality of
lateral openings;
an insulator lining said opening; and
a conductor filling said opening.

1 22. The integrated circuit in claim 21, wherein said lateral openings comprise
2 rectangular openings in cross-section.

1 23. The integrated circuit in claim 21, wherein said lateral openings comprise
2 v-shaped openings in cross-section.

1 24. The integrated circuit in claim 21, wherein said lateral openings comprise
2 rounded openings in cross-section.

1 25. The integrated circuit in claim 21, wherein said lateral openings increase a
2 surface area of said trench capacitor.

1 26. The integrated circuit in claim 21, wherein said lateral openings increase a
2 capacitance of said trench capacitor.

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